Abstracts

A phase-interpolation direct digital synthesizer with an adaptive integrator

A. Yamagishi, H. Nosaka, M. Muraguchi and T. Tsukahara. "A phase-interpolation direct digital synthesizer with an adaptive integrator." 2000 Transactions on Microwave Theory and Techniques 48.6 (Jun. 2000 [T-MTT] (Mini-Special Issue on the 1999 IEEE Radio and Wireless Conference (RAWCON))): 905-909.

A phase-interpolation direct digital synthesizer (DDS) with an adaptive integrator is described in this paper. Unlike a conventional DDS, it does not use ROM or a D/A converter. Therefore, less power is dissipated and the maximum speed is increased. The delay time for phase interpolation is generated by the adaptive integrator, which is composed of a capacitance switch array and current switch array, and by a comparator with constant threshold voltage. The DDS was fabricated on 0.5-/spl mu/m CMOS process technology. The spurious level is lower than -50 dBc and the power dissipation is 60 mW at a clock frequency of 40 MHz and output frequency of about 19 MHz.

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